

Rev 3.16 data - This table updated 16 June 2010.
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Artix™-7 FPGAs

Optimized for Lowest Cost and Power with Small Form-Factor Packaging
for the Highest Volume Applications (1.0 Volt, 0.9Volt)

Part Number		XC7A20	XC7A40	XC7A105	XC7A175T	XC7A355T
Logic Resources	Slices ⁽¹⁾	2,800	6,200	16,200	27,050	55,050
	Logic Cells ⁽²⁾	17,920	39,680	103,680	173,120	352,320
	CLB Flip-Flops	22,400	49,600	129,600	216,400	440,400
Memory Resources	Maximum Distributed RAM (Kbits)	225	450	1,275	2,063	4,188
	Block RAM/FIFO w/ ECC (36kbits each)	20	40	120	185	335
	Total Block RAM (Kbits)	720	1,440	4,320	6,660	12,060
Clock Resources	Mixed Mode Clock Managers (MMCM)	2	4	6	9	9
I/O Resources	Maximum Single-Ended I/O	100	200	300	450	450
	Maximum Differential I/O Pairs	48	96	144	216	216
Embedded Hard IP Resources	DSP48E1 Slices	40	80	240	400	700
	Gen1 PCI Express Interface Blocks	—	—	—	1	1
	Analog Front End (XADC) / SysMon Blocks	—	—	1	1	1
	Configuration AES / HMAC Blocks	—	—	1	1	1
	GTP 3.75Gpbs Transceivers	—	—	—	4	4
Speed Grades	Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3
	Industrial	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, 2
Configuration	Configuration Memory (Mbits)	5.2	10.4	27.0	45.0	84.6
Package ⁽⁴⁾		Area (Pitch)		Available User I/O: 3.3V SelectIO™ Pins ⁽³⁾ (GTP Transceivers)		
Wire bond, chip scale BGA (0.5mm ball spacing)						
CPG236		10 x 10 mm		100 (0)	140 (0)	140 (0)
Wire bond, chip scale BGA (0.8mm ball spacing)						
CSG324		15 x 15 mm			200 (0)	210 (0)
CSG484		19 x 19 mm			285 (0)	285 (4)
Wire bond, fine pitch BGA (1.0 mm ball spacing)						
FTG256		17 x 17 mm		100 (0)	170 (0)	
FGG484		23 x 23 mm			300 (0)	325 (0)
FGG784		29 x 29 mm				450 (4)

- Notes: 1. A single Artix-7 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops, for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
2. Artix-7 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
3. I/O standards supported: LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, 1.2V), HSTL_I (1.8V,1.5V), HSTL_II (1.8V,1.5V), Diff_HSTL_I (1.8V,1.5V), Diff_HSTL_II (1.8V), LVDS, Mini LVDS, PPDS, RSDS (pt-to-pt), SSTL_I (1.8V), SSTL_II (1.8V), SSTL (1.5V), PCI, TMDS
4. Contact Xilinx regarding available leaded package options.
5. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

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Kintex™-7 FPGAs
Optimized for Highest Price-Performance
(1.0 Volt, 0.9Volt)

	Part Number	XC7K30T	XC7K70T	XC7K120T	XC7K230T	XC7K410T					
Logic Resources	Slices ⁽¹⁾	4,750	10,550	18,350	35,550	63,550					
	Logic Cells ⁽²⁾	30,400	67,520	117,440	227,520	406,720					
	CLB Flip-Flops	38,000	84,400	146,800	284,400	508,400					
Memory Resources	Maximum Distributed RAM (Kbits)	413	838	1,500	3,038	5,663					
	Block RAM/FIFO w/ ECC (36kbits each)	65	135	225	445	795					
	Total Block RAM (Kbits)	2,340	4,860	8,100	16,020	28,620					
Clock Resources	Mixed Mode Clock Managers (MMCM)	3	6	8	10	10					
I/O Resources	Maximum Single-Ended I/O	150	300	400	500	500					
	Maximum Differential I/O Pairs	72	144	192	240	240					
Embedded Hard IP Resources	DSP48E1 Slices	120	240	400	840	1,540					
	Gen2 PCI Express Interface Blocks	1	1	1	1	1					
	Analog Front End (XADC) / SysMon Blocks	—	—	1	1	1					
	Configuration AES / HMAC Blocks	1	1	1	1	1					
	GTX 10.3125Gbps Transceivers	4	8	8	16	16					
Speed Grades	Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3					
	Industrial	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2					
Configuration	Configuration Memory (Mbits)	11.6	23.1	37.3	71.0	122.0					
Package ⁽⁵⁾		Area (Pitch)					Available User I/O: 3.3V capable SelectIO™ Pins⁽³⁾, 1.8V SelectIO Pins⁽⁴⁾ (GTX Transceivers)				
Lidless chip scale BGA supporting 6.6Gbps serial line rates (0.8mm ball spacing)											
SBG324		15 x 15 mm		100, 50 (4)		114, 50 (4)					
Lidless flip chip BGA supporting 6.6Gbps serial line rates (1.0mm ball spacing)											
FBG484		23 x 23 mm		100, 50 (4)		185, 100 (4)		185, 100 (4)			
FBG676		27 x 27 mm				200, 100 (8)		250, 150 (8)		250, 150 (8)	
FBG900		31 x 31 mm						350, 150 (16)		350, 150 (16)	
Flip chip BGA supporting 10.3Gbps serial line rates (1.0mm ball spacing)											
FFG676		27 x 27 mm				250, 150 (8)		250, 150 (8)		250, 150 (8)	
FFG900		31 x 31 mm						350, 150 (16)		350, 150 (16)	

- Notes: 1. A single Kintex-7 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops, for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
2. Kintex-7 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
3. I/O standards supported: LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, 1.2V), HSTL_I (1.8V, 1.5V), HSTL_II (1.8V, 1.5V), Diff_HSTL_I (1.8V, 1.5V), Diff_HSTL_II (1.8V), LVDS, Mini LVDS, PPDS, RSDS (pt-to-pt), SSTL_I (1.8V), SSTL_II (1.8V), SSTL (1.5V, 1.35V), PCI, TMDS
4. I/O standards supported: LVCMOS (1.8V, 1.5V, 1.2V), SSTL_I (1.8V), SSTL_I_DCI (1.8V), SSTL_II (1.8V), SSTL_II_DCI (1.8V), SSTL_II_T_DCI (1.8V), DIFF_SSTL_II_T_DCI (1.8V), DIFF_SSTL_I (1.8V), DIFF_SSTL_I_DCI (1.8V), DIFF_SSTL_II (1.8V), DIFF_SSTL_II_DCI (1.8V), HSTL_I (1.8V, 1.5V, 1.2V), HSTL_I_DCI (1.8V, 1.5V), HSTL_II (1.8V, 1.5V), HSTL_II_DCI (1.8V, 1.5V), HSTL_II_T_DCI (1.8V, 1.5V), DIFF_HSTL_II_T_DCI (1.8V, 1.5V), DIFF_HSTL_I (1.8V, 1.5V), DIFF_HSTL_I_DCI (1.8V, 1.5V), DIFF_HSTL_II (1.8V, 1.5V), DIFF_HSTL_II_DCI (1.8V, 1.5V), LVDCI (1.8V, 1.5V), HSTLVDCI (1.8V, 1.5V), LVDCI_DV2 (1.8V, 1.5V), SSTL (1.5V, 1.35V), SSTL_DCI (1.5V, 1.35V), DIFF_SSTL (1.5V, 1.35V), DIFF_SSTL_dci (1.5V, 1.35V), DIFF_SSTL_T_DCI (1.5V, 1.35V)
5. Contact Xilinx regarding available leaded package options.
6. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.

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Virtex®-7 FPGAs
Optimized for Highest System Performance and Capacity
(1.0 Volt, 0.9Volt)

	Part Number	XC7V285T	XC7V450T	XC7V585T	XC7V855T	XC7V1500T	XC7V2000T	XC7VX415T	XC7VX485T	XC7VX605T	XC7VX690T	XC7VX895T	XC7VX910T
Logic Resources	EasyPath™ Cost Reduction Solutions ⁽¹⁾	XCE7V285T	XCE7V450T	XCE7V585T	XCE7V855T	XCE7V1500T	XCE7V2000T	XCE7VX415T	XCE7VX485T	XCE7VX605T	XCE7VX690T	XCE7VX895T	XCE7VX910T
	Slices ⁽²⁾	44,700	70,450	91,050	133,350	229,050	305,400	64,400	75,900	94,800	107,800	139,600	142,200
	Logic Cells ⁽³⁾	286,080	450,880	582,720	853,440	1,465,920	1,954,560	412,160	485,760	606,720	689,920	893,440	910,080
	CLB Flip-Flops	357,600	563,600	728,400	1,066,800	1,832,400	2,443,200	515,200	607,200	758,400	862,400	1,116,800	1,137,600
Memory Resources	Maximum Distributed RAM (Kbits)	3,475	5,388	6,938	10,313	16,163	21,550	6,525	8,000	9,150	10,850	13,525	13,725
	Block RAM/FIFO w/ ECC (36kbits each)	410	615	795	1,155	1,155	1,540	880	1,030	1,200	1,460	1,740	1,800
	Total Block RAM (Kbits)	14,760	22,140	28,620	41,580	41,580	55,440	31,680	37,080	43,200	52,560	62,640	64,800
Clock Resources	Mixed Mode Clock Managers (MMCM)	14	14	18	18	18	24	12	14	12	20	18	18
I/O Resources ^(4, 5)	Maximum Single-Ended I/O	700	700	850	850	850	1200	600	700	600	1,000	880	640
	Maximum Differential I/O Pairs	336	336	408	408	408	576	288	336	288	480	422	307
Embedded Hard IP Resources	DSP48E1 Slices	700	980	1,260	1,800	1,620	2,160	2,160	2,800	2,640	3,600	3,960	3,960
	Gen2 PCI Express Interface Blocks	2	3	3	3	3	4	—	4	—	—	—	—
	Analog Front End (XADC) / SysMon Blocks	1	1	1	1	3	4	1	1	2	1	3	3
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1	1	1
	GTX 10.3125Gbps Transceivers	28	28	36	36	36	36	24	56	—	56	48	—
	GTH 13.1Gbps Transceivers	—	—	—	—	—	—	24	—	48	24	24	72
Speed Grades	Commercial	-1L, -1, -2, -3	-1L, -1, -2, -3	-1L, -1, -2, -3	-1L, -1, -2, -3	-1L, -1, -2	-1L, -1, -2	-1, -2, -3	-1, -2, -3	-1, -2	-1, -2, -3	-1, -2	-1, -2
	Industrial	-1L, -1, -2, -3	-1L, -1, -2, -3	-1L, -1, -2	-1L, -1, -2	-1L, -1	-1L, -1	-1, -2	-1, -2	-1	-1, -2	-1	-1
Configuration	Configuration Memory (Mbits)	75.3	115.4	148.3	214.9	323.0	430.6	127.0	150.0	177.0	212.0	267.0	266.0
Package ⁽⁶⁾		Area		Available User I/O: 3.3V capable SelectIO™ Pins ⁽⁴⁾, 1.8V SelectIO Pins ⁽⁵⁾ (GTX Transceivers)				Available User I/O: 1.8V SelectIO™ Pins ⁽⁵⁾ (GTX, GTH Transceivers)					
Flip chip, fine pitch BGA (1.0 mm ball spacing)													
	FFG484	23 x 23 mm	0, 250 (8)										
	FFG784	29 x 29 mm	50, 350 (12)	50, 350 (12)					400 (12, 0)				
	FFG1157	35 x 35 mm	0, 600 (20)	0, 600 (20)	0, 600 (20)	0, 600 (20)	0, 600 (20)		600 (20, 0)				
	FFG1761	42.5 x 42.5 mm	50, 650 (28)	50, 650 (28)	100, 750 (36)	100, 750 (36)	0, 850 (36)	0, 850 (36)	700 (28, 0)				
	FFG1925	45 x 45 mm					1200 (16)						
	FFG1158	35 x 35 mm							320 (48, 0)		320 (48, 0)		
	FFG1159	35 x 35 mm						320 (24, 24)			320 (24, 24)		
	FFG1926	45 x 45 mm						600 (24, 24)			640 (48, 24)	640 (48, 24)	
	FFG1927	45 x 45 mm									880 (24, 24)	880 (24, 24)	
	FFG1928	45 x 45 mm								600 (0, 48)			640 (0, 72)
	FFG1929	45 x 45 mm							560 (56, 0)		560 (56, 24)		
	FFG1930	45 x 45 mm									1000 (28, 0)		

- Notes: 1. EasyPath™ solutions provide a conversion-free, low-risk path for volume production
2. A single Virtex-7 FPGA CLB comprises two slices, with each containing four 6-input LUTs and eight Flip-Flops, for a total of eight 6-LUTs and 16 Flip-Flops per CLB.
3. Virtex-7 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
4. I/O standards supported: LVCMOS (3.3V, 2.5V, 1.8V, 1.5V, 1.2V), HSTL_I (1.8V, 1.5V), HSTL_II (1.8V, 1.5V), Diff_HSTL_I (1.8V, 1.5V), Diff_HSTL_II (1.8V), LVDS, Mini LVDS, PPDS, RSDS (pt-to-pt), SSTL_I (1.8V), SSTL_II (1.8V), SSTL (1.5V, 1.35V), PCI, TMDS
5. I/O standards supported: LVCMOS (1.8V, 1.5V, 1.2V), SSTL_I (1.8V), SSTL_I_DCI (1.8V), SSTL_II (1.8V), SSTL_II_DCI (1.8V), SSTL_II_T_DCI (1.8V), DIFF_SSTL_II_T_DCI (1.8V), DIFF_SSTL_I (1.8V), DIFF_SSTL_I_DCI (1.8V), DIFF_SSTL_II (1.8V), DIFF_SSTL_II_DCI (1.8V), HSTL_I (1.8V, 1.5V, 1.2V), HSTL_I_DCI (1.8V, 1.5V), HSTL_II (1.8V, 1.5V), HSTL_II_DCI (1.8V, 1.5V), HSTL_II_T_DCI (1.8V, 1.5V), DIFF_HSTL_II_T_DCI (1.8V, 1.5V), DIFF_HSTL_I (1.8V, 1.5V), DIFF_HSTL_I_DCI (1.8V, 1.5V), DIFF_HSTL_II (1.8V, 1.5V), DIFF_HSTL_II_DCI (1.8V, 1.5V), LVDCI (1.8V, 1.5V), HSTLVDCI (1.8V, 1.5V), LVDCI_DV2 (1.8V, 1.5V), SSTL (1.5V, 1.35V), SSTL_DCI (1.5V, 1.35V), DIFF_SSTL (1.5V, 1.35V), DIFF_SSTL_dci (1.5V, 1.35V), DIFF_SSTL_T_DCI (1.5V, 1.35V)
6. Contact Xilinx regarding available leaded package options.
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